Abstract of the Disclosure

Provided are a semiconductor memory device with a column select line (CSL) driving scheme capable of reducing skew between column select lines, and a CSL driving method. The semiconductor memory device includes a plurality of CSL enable controllers and a plurality of CSL disable controllers that are installed around corresponding CSL drivers, thereby making loads on input terminals of the CSL drivers almost the same and reducing enable and disable skew between the CSLs. The semiconductor memory device includes a plurality of enable master signal delayers that delay a signal output from a CSL enable master signal generator for different times so as to generate different delay signals and transmit the delay signals to the plurality of CSL enable controllers, and a plurality of disable master signal delayers that delay a signal output from a CSL disable master signal generator for different times so as to generate different delay signals and transmit the delay signals to the plurality of CSL disable controllers. Accordingly, it is possible to compensate for signal delay caused by different loads on signal transmission lines and further reduce enable and disable skew between the CSLs.

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